IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Thomas A. Figura et al.	§	Group Art Unit: 2829
		§	
		§	
		§	Examiner: Lisa Kilday
Serial No:	09/470,650	§	
		§	Atty. Docket: 94-0280.04
Filed:	December 22, 1999	§	
		§	
For: USE OF A PLASMA SOURCE TO FORM A LAYER DURING THE FORMATION OF A SEMICONDUCTOR DEVICE		§	

APPLICANTS' BRIEF ON APPEAL

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Date 3/24/03

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APPLICANTS' BRIEF ON APPEAL

I. REAL PARTY IN INTEREST

The Applicants, Thomas Figura, Kevin Donohoe, and Thomas Dunbar have assigned their interest in this application to Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are other appeals or interferences known to the Applicants or the assignee which may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

The application under appeal shares a common parent application with U.S. App. Ser. No. 09/471,460 (both are divisionals of U. S. App. Ser. No. 09/046,835, filed Oct. 24, 1997 and issued as U.S. Pat. No. 6,117,764). In prosecuting application '460, Applicants filed an Appeal Brief on Jan. 20, 2003. However, in a Mar. 5, 2003 telephone conversation between Applicants' attorney and the Examiner, the Examiner indicated that the claims would be allowable after an Examiner's amendment agreed to by Applicants' attorney.

The application under appeal also shares its parent with U.S. App. Ser. No. 09/470,651 (a continuation application). Applicants' latest act during prosecution of application '651 was to file an Appeal Brief on Mar. 7, 2003.

III. STATUS OF THE CLAIMS

Claims 1-46 have been presented during prosecution of the application under appeal.

Claims 9, 15-18, 20-22, 25-28, 33-35, and 44-46 have been cancelled.

Claims 1-8, 10-14, 19, 23-24, 29-32, and 36-43 are pending.

Claims 1-8, 10-14, 19, 23-24, 29-32, and 36-43 are rejected.

Claims 1-8, 10-14, 19, 23-24, 29-32, and 36-43 are appealed.

IV. STATUS OF THE AMENDMENTS

Applicants filed no amendments subsequent to the latest rejection.

V. SUMMARY OF THE INVENTION

Exemplary embodiments of the current invention concern the use of a plasma source to form a layer during the formation of a semiconductor device. At least one exemplary embodiment is directed to a method of depositing a polymer onto a wafer, comprising several acts. One such act is defining an opening. (Specification at p. 5, ln. 1 and Fig. 1 (describing and illustrating a formed contact).) The opening is between exposed metal protruding features on the wafer. (***Id***. at p. 4, ln. 17-18 (noting that the invention can be used to form a number of structures); p. 9, ln. 21 – p. 10, ln. 3 (indicating that the recess for a polymer can be "any recess" and can be formed between two protruding features and in layers other than an oxide; p. 8, ln. 14 (disclosing conductive material); FIGS. 5-6).) Another act in the method is providing a plasma. (***Id***. at p. 7, ln. 16-18 (disclosing a combination of settings in a chamber of a plasma source).) Yet another act is exposing the opening to the plasma. (***Id***. at p. 7, ln. 17-19 (disclosing that the combination of settings forms an etch resistant layer within the contact or other opening).) In a narrower embodiment of this type, the act of providing the plasma comprises providing a high-density plasma. (***Id***. at p. 5, ln. 12, 14-15, 17 (referring to "HDP"); p. 8, ln. 2); *see also* specification of U.S. App. Ser. No. 08/458,861 (great grandparent of the appealed application) at p. 6, ln. 8, 11, 13; p. 9, ln. 15.)

VI. ISSUES

There are three issues for determination on appeal.

1. Whether the Specification provides support satisfying the requirements of 35 U.S.C. §112, ¶1.

2. Whether the Examiner has cited inappropriate art for the 35 U.S.C. §102 rejections.

3. Whether the Examiner has cited inappropriate art for the 35 U.S.C. §103 rejections.

VII. GROUPING

Applicants define the following groups of claims for consideration upon this appeal. These groups correspond to the issues listed above.

Group I: claims 1-8, 10-14, 19, 23-24, 29-32, and 36-43;

Group II: claims 1-3, 7, 13, and 36-38; and

Group III: claims 1-6, 8, 10-12, 14, 19, 23-24, 29-32, 39-43.

VIII. ARGUMENT:

The Examiner rejected the claims under either §112, §102, or §103. Applicants address each basis for rejection separately below.

A. The Specification provides support satisfying the requirements of 35 U.S.C. §112, ¶1.

The Examiner rejected claims 1-8, 10-14, 19, 23-24, 29-32, and 36-43 under 35 U.S.C. §112 ¶1, arguing that the claims contained subject matter insufficiently described in the specification. The Examiner admitted that the formation of a polymer is described. (Office Action dated 10/24/02 at p. 2, ln. 4; p. 3, ln. 23.) Nevertheless, the Examiner supported the rejection based on the assumption that the specification of the current application's great grandparent does not disclose polymer formation by high density plasma (HDP). (***Id***. at p. 2-3.)

First, Applicants note that not all of the claims include high density plasma limitations. Specifically, such limitations are not included in claims 7-13, 19, 23- 24, 36-38, and 40-43. As a result, the Examiner's basis for rejection under §112 does not apply to these claims. Moreover, the Examiner's admission regarding polymer formation indicates that those claims satisfy §112. Second, Applicants contend that the Examiner's assumption regarding the grandparent's disclosure is incorrect. Applicants direct the Board to page 6, lines 8 and 11, of the great

grandparent's specification, which expressly refer to "high density plasma" multiple times. Moreover, page 6, line 13 and page 9, line 15 of the great grandparent's specification express the term "HDP," which is understood to stand for "high density plasma." (A copy of the great grandparent's specification – U.S. App. Ser. No. 08/458,861 – is included in an appendix to this Appeal Brief.) Applicants contend that such explicit references refute the Examiner's basis for rejection and warrant the Board's reversal of the Examiner and withdrawal of the §112 rejections.

B. The Examiner has cited inappropriate art for the 35 U.S.C. §102 rejections.

The Examiner rejected claims 1-3, 7, 13, and 36-38 as being anticipated by an article from John Arnold that was not published until 10/21/96. (Office Action dated 10/24/02 at p. 3-4.) Presumably the Examiner found such a late publishing date to be sufficient based on the Examiner's belief that the appealed application is not entitled to the priority date of its great grandparent, filed 6/2/95. (*See* Office Action dated 10/24/02 at p. 2.) That belief, in turn, is based on the assumption that the great grandparent's Specification does not disclose forming a polymer in a high density plasma environment. (***Id.***) However, Applicants have refuted this assumption in part A above. Hence, the appealed claims are entitled to the benefit of the great grandparent's priority date, and the Arnold publication cannot serve as prior art. Accordingly, Applicants request that the Board reverse the Examiner and withdraw the §102 rejections.

C. The Examiner has cited inappropriate art for the 35 U.S.C. §103 rejections

The Examiner rejected claims 4-6, 8, 10-12, 19, 23-24, 29-32, and 39-43 as obvious in light of the Arnold publication in combination with Nulty (U.S.Pat. No. 5,562,801). However, as established above, (1) the current application is entitled to the benefit of the priority date of its great grandparent application – filed 6/2/95; and (2) Arnold was not published until 10/21/96. As a result, one of the references in the relied upon combination is not prior art, and the obviousness rejection fails accordingly.

Similarly, the Examiner rejected claims 1-6, 14, 24, 29-32, and 39 as obvious in light of Robles (U.S.Pat. No. 5,804,259). However, Robles was filed on 11/7/96. As established above,

the current application benefits from the priority date of its great grandparent application – filed 6/2/95. Hence, Robles cannot be considered prior art.

Applicants submit that the Examiner's reliance on non-prior art references to support the obviousness rejections supports the Board's reversal the Examiner and withdrawal the §103 rejections.

D. The Examiner's response to Applicants' previous arguments fails to support the current rejections.

In the interest of fully responding to the points raised in the Examiner's Office Action dated 10/24/02, Applicants note that the page 7 of that Office Action contains text purporting to respond to Applicants' previous arguments. In the first paragraph of that section, the Examiner begins with a reference to overcoming "the 101 rejection." However, Applicants cannot find an express citation to 35 U.S.C. §101 as a basis for rejection in the previous Office Action. (*See* Office Action dated 3/15/02 (citing only §112, §102, and the judicially-created rejection of obviousness-type double patenting as bases for rejection).) The other two sentences in the Examiner's first paragraph appear to only recite text of the Specification.

In the second paragraph of the Examiner's response, the Examiner attempts to restate Applicants' argument and concludes that Applicants' citations to the Specification support etching, not forming a polymer. However, a careful reading of the previously cited excerpts demonstrates that the Specification expressly discloses that a "layer of etch resistant material 22, such as a polymer, is formed." (Appealed Specification at p. 5, ln. 17-18; *see also* p. 6, ln. 13-14.) Moreover, the text immediately surrounding these excerpts addresses parameters for accomplishing the formation of the polymer. Applicants conclude that the Examiner's attempts at responding to previously-raised arguments are either irrelevant or have been refuted by the express language of the Specification.

E. Conclusion

Sufficient description of the claimed embodiments can be found in the current specification as well as every other specification in the appealed application's family extending

as far back as the original application filed 6/2/95. As a result, the appealed application enjoys the benefit of the priority established by the original application. Moreover, because the Examiner's §102 and §103 rejections depend upon an article published or a patent filed after 6/2/95, the Examiner's rejections fail. Further, the Examiner's response to Applicants' previous arguments fail to cure the defective rejections. Accordingly, Applicants request that the Board reverse the Examiner, withdraw the rejections, and allow the claims.

Respectfully submitted,

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Appendix 1: Copy of Involved Claims

1. A method of forming a semiconductor device, comprising:

providing a surface within said semiconductor device;

providing a first feature on said surface;

providing a second feature on said surface; and

forming a polymer between said first feature and said second feature in a high-density plasma environment.

2. The method in claim 1, further comprising modifying said polymer within said high-density plasma environment.

3. The method in claim 2, wherein said step of modifying said polymer further comprises etching a portion of said polymer.

4. The method in claim 3, wherein said step of providing a first feature further comprises providing a first metallic feature; and providing a second feature further comprises providing a second metallic feature.

5. The method in claim 4, wherein said step of providing a first feature further comprises providing a first feature made of a metal; and providing a second feature further comprises providing a second feature made of said metal.

6. The method in claim 5, wherein said step of providing a first feature further comprises providing a first metal line; and providing a second feature further comprises providing a second metal line.

7. A method of processing a semiconductor device, comprising:

providing a first protruding feature on a layer of said semiconductor device;

providing a second protruding feature on said layer;

defining a recess between said first protruding feature and said second protruding feature; and

plasma-depositing a material within said recess.

8. The method in claim 7, wherein said step of plasma-depositing a material further comprises plasma-depositing a material comprising carbon and a halogen.

10. The method in claim 7, wherein said step of plasma-depositing a material further comprises plasma-depositing a material comprising carbon and hydrogen.

11. The method in claim 10, wherein said step of plasma-depositing a material further comprises plasma-depositing a halogen-free material.

12. The method in claim 7, wherein said step of plasma-depositing a material further comprises depositing a material comprising carbon, a halogen, and hydrogen.

13. A method of depositing a polymer onto a wafer, comprising:

defining an opening between exposed metal protruding features on said wafer;

providing a plasma; and

exposing said opening to said plasma.

14. The method in claim 13, wherein said step of providing said plasma further comprises providing a high-density plasma.

19. A method of providing a polymer between metal lines on a wafer, comprising:

providing a plasma source;

exposing said wafer to said plasma source;

introducing a feed gas to said wafer;

establishing a pressure around said wafer; and

forming said polymer between said metal lines using said feed gas.

23. A method of forming a polymer, comprising:

providing a semiconductor device having at least two exposed metal lines; and

performing a process on said semiconductor device, wherein said process is

defined by a plurality of parameters, comprising:

a source power magnitude,

a bias power magnitude,

a pressure,

a duration, and

a process gas flow rate.

24. The method in claim 23, wherein said step of performing said process further comprises:

providing a high-density plasma etcher having a plurality of process settings, comprising:

a source power setting,

a bias power setting,

a pressure setting,

a duration setting, and

a process gas flow rate setting; and

placing said semiconductor device in said etcher.

29. A method of selectively forming a polymer, comprising:

providing a semiconductor device having a plurality of exposed protruding features;

providing an etcher having high-density plasma process settings, comprising:

a source power setting,

a bias power setting, and

a flow rate setting; and

exposing said semiconductor device to a high-density plasma process within said etcher.

30. The method in claim 29, further comprising:

defining at least one recess with said plurality of exposed protruding features;

filling said recess with said polymer; and

restricting formation of said polymer to within said recess.

31. The method in claim 30, wherein said step of defining at least one recess with said plurality of exposed protruding features comprises defining a recess between two protruding features of said plurality of protruding features.

32. The method in claim 31, wherein said step of restricting formation of said polymer to within said recess further comprises preventing a formation of said polymer above said two protruding features.

36. A method of selectively providing a material between two metal lines of a semiconductor device, comprising:

forming said material on said semiconductor device in a deposition environment; and

removing any excess of said material in an etching environment, wherein said etching environment is the same as said deposition environment.

37. The method in claim 36, wherein said step of forming said material further comprises forming said material in an etch chamber.

38. The method in claim 36, wherein said step of removing any excess of said material further comprises removing any excess of said material in a plasma deposition chamber.

39. A method of processing a wafer having metal lines, comprising:

providing a high-density plasma; and

forming a polymer between said metal lines using said high-density plasma.

40. A method of developing an in-process semiconductor device having a first metal line and a second metal line, comprising:

placing said device in a deposition and etch surrounding; and

forming a polymer between said first metal line and said second metal line.

41. The method in claim 40, further comprising:

providing a layer over said polymer; and

retaining a state of said polymer.

42. The method in claim 41, wherein said step of retaining said state of said polymer further comprises having a polymer with a thermal stability sufficient to withstand providing said layer.

43. The method in claim 42, wherein said step of providing said layer further comprises providing said layer outside of said deposition and etch surrounding.

Appendix 2:

Specification of U.S. App. Ser. No. 08/458,861 (great grandparent of the application under appeal)

Abstract

A method used to form a semiconductor device having a capacitor comprises placing a semiconductor wafer assembly into a chamber of a plasma source, the wafer assembly comprising a layer of insulation having at least one contact therein and a surface, and further comprising a conductive layer over the surface and in the contact. Next, in the chamber, a layer of etch resistant material is formed within the contact over the conductive layer, the etch resistant material not forming over the surface.

USE OF A PLASMA SOURCE TO FORM A LAYER DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

Field of the Invention

The invention relates to the field of semiconductor manufacture, and more specifically to a method for forming and etching layers during the formation of a semiconductor device.

Background of the Invention

A typical structure formed during the manufacture of a semiconductor memory device is a container cell which requires several steps for its manufacture. A sample process for forming the container cell includes implanting a diffusion area in a semiconductor wafer substrate, and forming an insulator, such as borophosphosilicate glass (BPSG) or tetraethylorthosilicate (TEOS), over the wafer. The insulator is etched to open a contact, usually round or oval in shape, to expose the diffusion region. A compliant conductive layer such as doped polycrystalline silicon is formed over the wafer surface and within the contact which contacts the

diffusion region. The conductive layer is masked to protect the portion within the contact and the remainder is etched. Various steps as known in the art are subsequently performed to produce a container cell.

The process described above requires the wafer to be transported between several chambers. The diffusion region is formed in an implanter, and the insulator, usually a blanket layer, is formed either in a furnace (to form TEOS) or in a chemical vapor deposition tool such as a Watkins-Johnson to form BPSG. Plasma-enhanced chemical vapor deposition (PECVD) and various other means can be used to form the insulator. The wafer is then moved to a stepper for patterning of the insulator, then to a dry etch chamber where the insulator is etched to form the contact. The wafer is moved again to a furnace, a low-pressure chemical vapor deposition (LPCVD) chamber, or a PECVD chamber to form a blanket conductive layer over the wafer surface and within the contact. Next, the conductive layer on the surface of the wafer is removed, for example using chemical mechanical planarization (CMP) equipment. The conductive layer can also be removed by forming a resist coat over the wafer, which forms a thicker layer within the contact

than on the wafer surface, and dry etching the surface to remove the resist and poly from the surface while leaving a portion of the poly within the contact. Finally, the wafer is moved to an acid bath or a plasma etcher where the resist is stripped from the contact.

Transporting the wafer is not desirable as it increases processing time, costs, and possible damage and contamination to the wafer. A process which requires less wafer transportation is therefore desirable.

Summary of the Invention

A first embodiment of the invention is a method used during the formation of a semiconductor device comprising placing a semiconductor wafer having a surface and a recess formed in the wafer into a chamber of a plasma source. Within the chamber, a layer of etch resistant material is formed within the recess and over the surface of the wafer. Finally, also in the chamber, the etch resistant layer which forms over the surface of the wafer is removed and at least a portion of the etch resistant layer is left in the recess.

A second embodiment of the invention comprises a method used during the formation of a semiconductor device comprising placing a semiconductor wafer having a surface and a recess formed in the wafer into a chamber of a plasma source. Within the chamber, a layer of etch resistant material is formed within the recess, the etch resistant material not forming over the surface.

Objects and advantages will become apparent to those skilled in the art from the following detailed description read in conjunction with the appended claims and the drawings attached hereto.

Brief Description of the Drawings

FIGS. 1-4 are cross-sections of a first embodiment of the invention;

FIGS. 5-6 are cross-sections of a second embodiment of the invention; and

FIGS. 7-8 are cross-sections of a third embodiment of the invention.

It should be emphasized that the drawings herein are not to scale but are merely schematic representations and are not intended to portray the specific parameters or the structural details of the invention, which can be determined by one of skill in the art by examination of the information herein.

Detailed Description of the Invention

FIGS. 1-4 are cross-sections of a first embodiment of the invention used to form a storage node of a container cell. It should be noted that the invention can be used to form a number of other structures, and the use of the invention to form a storage node of a container cell is for ease of explanation.

A starting structure is shown in FIG. 1. The starting structure comprises a wafer 10 having a surface 12 and a contact 14 formed in the wafer. The wafer shown comprises a substrate 16, for example of silicon or gallium arsenide, and insulator 18, such as an oxide or a nitride, with the contact formed in the insulator. The specific use of the invention shown further comprises a conductive layer 20 such as a conformal layer of polycrystalline silicon formed within the contact 14 and over the wafer surface 12 which contacts the substrate 16. The invention is

described for a starting structure using a 1,000Å to 20,000Å thick BPSG layer as the insulator, a contact 0.2 to 1.0 microns in diameter, and a polycrystalline silicon conductor layer 200-2,000Å thick. Etcher settings listed below may require modification for different materials and/or thicknesses, which can easily be determined by one of ordinary skill in the art from the description herein without undue experimentation.

The structure of FIG. 1 is placed into a chamber of a plasma source such as a conventional plasma etcher or a high density plasma etcher. High density plasma etchers operate at pressures below 50 millitorr (typically below 10 millitorr) and have plasma densities greater than 10^{10} to 10^{11} cm^{-3}. In addition, most etch applications of high density plasma etchers use two sources of electrical power, one to generate the plasma and one to bias the wafer. The plasma source can be an etcher such as an Applied Materials Model 5300 HDP, LAM TCP, or other such etcher. A layer of etch resistant material 22, such as a polymer, is formed within the contact 14 and over the surface 12 of the wafer 10 as shown in FIG. 2. The etch resistant material bridges across the contact and fills in the contact. In general, any feed gas which forms an etch resistant layer can be used. For example, fluorocarbons, hydrofluorocarbons, chlorofluorocarbons, halocarbons or

hydrohalocarbons would function sufficiently. Examples include CHF_3, CH_2F_2, C_2F_6, C_2HF_5, C_3F_8. The flow rate depends on which feed gas is used, and can be determined by one of skill in the art from the description herein without undue experimentation. Generally, flow rates would generally be in the range of 25-200 standard cubic centimeters (sccm) although flow rates outside this range may function adequately. To bridge over a contact 0.5 microns in diameter and form a polymer layer about 2000 angstroms (Å) thick over the wafer surface, the following settings can be used:

Source (top) Power: From 1000 to 3500 Watts
Bias (bottom) Power: From 0 to 400 Watts
Pressure: From 2 to 5 Millitorr
Duration: From 5 to 40 Seconds
Flow Rate: From 10 to 50 SCCM

These settings usually cause the etch resistant layer formed on the surface to be thinner than the material formed within the contact. It should be noted that there is an interaction between the listed parameters, and other settings in addition to the ranges listed above may also function adequately. The setting herein can be altered by one of ordinary skill in the art from the description herein to customize the etch resistant layer formation for various sizes and shapes of contact, and for various thicknesses within the contact and over the wafer surface. Depending on the

application, any thickness of etch-resistant layer may be useful, but an etch-resistant layer 50Å or greater is preferred for most applications.

Next, within the chamber, the etch resistant layer is removed from the wafer surface as shown in FIG. 3 using parameters known in the art. Because the etch resistant layer bridges across the contact, and essentially forms a thicker layer within the contact, the layer can be removed from the surface while at least a portion 30 of the layer remains within the contact as shown in FIG. 3. In addition, the portion of the conductive layer 20 on the wafer surface 12 can also be removed using the same settings used to remove the etch resistant layer from the wafer surface, or different settings can be used depending on the material of layer 20. The remaining portion of the etch resistant layer 30 functions as a mask to protect the conductive layer 32 within the contact.

The etch resistant layer 30 can be removed, for example within the chamber, to expose the conductive layer 32 to result in the structure of FIG. 4. The etch resistant layer 30 can be removed using etcher settings similar to those used for stripping photoresist. Oxygen-fluorocarbon mixtures are best suited for this since layer 30 may comprise some silicon. Using subsequent processing steps element 32 can

function as a capacitor storage node, although there are many other uses for the inventive method. Removal of insulator 18 can be accomplished with any means, such as within the etch chamber or outside the chamber, for example in a hydrofluoric acid (HF) sink.

A second embodiment of the invention is shown in FIGS. 5 and 6. The starting structure of FIG. 1 is placed into a chamber of a plasma source. Using a combination of etcher settings, an etch resistant layer 50 can be formed within the contact 14, or other narrow openings, without the etch resistant layer forming on the wafer surface 12 to result in the structure of FIG. 5. The thickness of the etch resistant layer which forms within the contact is dependent on the duration of the step. As the layer thickens its rate of formation slows and may eventually stop. Forming the etch resistant layer in the contact and not on the wafer surface results in part from operating at a higher bias voltage and under conditions of lower deposition rate than in the first embodiment. For example, in the Applied Materials HDP Etch tool, these conditions would include lowering the source power and decreasing the total flow rate of process gasses. The specific values of the operating parameters can be adjusted by one of skill in the art from the information herein.

The etch resistant layer can then be used as a mask and the conductive layer 20 can be etched with a separate etch step, for example in the same etch chamber, according to means known in the art. Next, the etch resistant layer 50 can be removed as described with the first embodiment above to result in the structure of FIG. 4.

A third embodiment of the invention is shown in FIGS. 7-8. The starting structure of FIG. 7 is placed in an etch chamber. By decreasing the deposition rate and increasing the bias of the settings shown for the first embodiment, an etch resistant layer 80 can be formed within the contact 14 while, simultaneously, the conductive layer 20 is etched from the surface of the wafer. As the polymer builds up over the conductive layer 20 within the contact 14, it functions as a mask and protects the horizontal surface of the conductive layer in the contact. The conductive layer is simultaneously removed from the surface of the wafer. Some attack on the top of 20 may occur with this embodiment, but such an attack does not affect the performance of the container cell.

The inventive method as described in the embodiments above has the advantage of forming a mask in an etch chamber. Subsequent etches can also be performed within the chamber. Performing a number of different steps within the etch chamber decreases the transportation requirements of the wafer which reduces production time and decreases damage resulting from handling of the wafers.

The three embodiments described have various deposition rates of the polymer on the wafer surface compared with the deposition rate of the polymer within the recess. With the first embodiment, the polymer forms faster within the recess than on the wafer surface. In the second embodiment, the polymer does not form on the wafer surface but forms within the recess. In the third embodiment, an etch occurs on the wafer surface while the polymer forms within the recess. The deposition rate of the polymer on the wafer surface can be decreased as compared to the polymer formation within the recess by various means, such as by decreasing the source power, by decreasing the flow rate, by increasing the bias power, or by using a combination of these parameters. Other methods of controlling the deposition rate may also be possible and apparent to one of skill in the art from reviewing the information herein. These other methods fall within the scope of the invention.

While this invention has been described with reference to illustrative embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as additional embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. For example, the etch resistant layer can be formed within any recess such as a trench, via, contact, depression in an exposed surface with modifications to the etcher settings. Depending on the size of the recess, the etcher settings may require modification, which can be determined without undue experimentation from the disclosure herein. Also, the recess can be formed in an oxide layer as shown herein, or can be formed within the wafer substrate, between two protruding features, or in other layers. The term "wafer assembly" is used to describe a raw substrate, a substrate with doped regions therein, or a substrate with a layer or layers such as oxide or nitride thereon. Further, "polymer" is intended to describe any plasma-deposited material, including (but not limited to) those materials comprising carbon and either or a halogen and/or hydrogen. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

Claims

What is claimed is:

1. A method for forming a semiconductor device, comprising the steps of:

a) placing a semiconductor wafer assembly into a chamber of a plasma source, said wafer assembly comprising a surface and at least one recess formed in said wafer assembly;

b) in said chamber, forming a layer of etch resistant material within said recess and over said surface; and

c) in said chamber, removing said etch resistant layer which forms over said surface and leaving at least a portion of said etch resistant layer in said recess.

2. The method of claim 1, further comprising:

d) in said chamber subsequent to said removing said etch resistant layer which forms over said surface, performing an etch using said etch resistant layer in said recess as a mask.

3. The method of claim 2 further comprising forming a conductive layer over said surface between said step of placing said wafer assembly in said chamber and said step of forming said layer of etch resistant material, and wherein said step of performing said etch removes said conductive layer and said etch resistant layer from over said surface and leaves at least a portion of said conductive layer and said etch resistant layer in said recess.

4. The method of claim 2, further comprising the step of:

e) removing said etch resistant material from said recess subsequent to said step of performing said etch.

5. The method of claim 4, wherein said step of removing said etch resistant material from said recess is performed in said chamber.

6. The method of claim 1 wherein said etch resistant layer comprises a polymer.

7. The method of claim 1 wherein said wafer assembly comprises a layer of oxide, and wherein said recess is formed in said oxide layer.

8. A method of forming a capacitor storage node, comprising the steps of:

a) placing a semiconductor wafer assembly into a chamber of a plasma source, said wafer assembly comprising at least one contact therein, a surface, and a layer of capacitor storage node material;

b) in said chamber, forming a layer of etch resistant material over said capacitor storage node material, said etch resistant material formed with a greater thickness in said contact than over said surface.

9. The method of claim 8 wherein said etch resistant layer forms over said surface during said step of forming said etch resistant material, further comprising the step of:

c) in said chamber, removing said etch resistant layer which forms over said surface and leaving a portion of said etch resistant layer in said contact.

10. The method of claim 8 wherein said surface remains free of said etch resistant layer during said step of forming said etch resistant material.

11. The method of claim 8, further comprising the step of:

c) in said chamber, etching said storage node material using said etch resistant layer as a mask, said etching removing said storage node material from said surface and leaving at least a portion of said storage node material in said contact.

12. The method of claim 11 wherein said etch resistant layer forms over said storage node material and said surface during said step of forming said etch resistant material, and said etching removes said etch resistant layer from over said surface.

13. The method of claim 11, further comprising the step of:

d) removing said etch resistant material from said contact subsequent to said step of etching said storage node material.

14. The method of claim 13, wherein said step of removing said etch resistant material from said contact is performed in said chamber.

15. The method of claim 8 wherein said etch resistant layer comprises a polymer.

16. The method of claim 8 wherein said wafer assembly comprises a layer of oxide, and said contact is formed in said oxide layer.

17. A method of forming a container capacitor during the formation of a semiconductor device comprising the steps of:

a) placing a semiconductor wafer assembly into a chamber of a plasma source, said wafer assembly comprising at least one contact therein having a sidewall and a bottom, said wafer assembly further comprising a surface and a layer of capacitor electrode material over said surface, said contact bottom, and said contact sidewall;

b) in said chamber, forming a polymer over at least a portion of said capacitor material, said polymer formed with a greater thickness in said contact than over said surface;

c) etching said capacitor material using said polymer as a mask.

18. The method of claim 17 wherein said polymer forms over said surface during said step of forming said polymer, further comprising:

d) in said chamber, removing said polymer which forms over said surface and leaving at least a portion of said polymer in said contact.

19. The method of claim 17 wherein said surface remains free of said polymer during said step of forming said polymer.

20. The method of claim 17 wherein said etching step removes said storage node material from said surface and leaves at least a portion of said storage node material in said contact.

21. The method of claim 20 wherein said polymer forms over said storage node material and said surface during said step of forming said polymer, and said step of etching removes said polymer from said surface.

22. The method of claim 20, further comprising:

d) removing said polymer from said contact subsequent to said step of etching.

23. The method of claim 22, wherein said step of removing said polymer from said contact is performed in said chamber.

24. The method of claim 17 wherein said wafer assembly comprises a layer of oxide, and said contact is formed in said oxide layer.

25. A method of forming a semiconductor device, comprising:

a) placing a semiconductor wafer assembly into a chamber of a plasma source, said wafer assembly comprising a surface and at least one recess formed in said wafer assembly;

b) in said chamber, forming a layer of etch resistant material within said recess, said surface remaining free of said etch resistant material.

26. The method of claim 25, further comprising:

c) in said chamber, performing an etch using said etch resistant layer as a mask.

27. The method of claim 26, further comprising:

d) removing said etch resistant material from said recess subsequent to said step of performing said etch.

28. The method of claim 27, wherein said step of removing said etch resistant material from said recess is performed in said chamber.

29. The method of claim 25 further comprising forming a conductive layer over said surface between said step of placing said wafer assembly in said chamber and said step of forming a layer of etch resistant material within said recess, and wherein said step of forming a layer of etch resistant material removes said conductive layer from over said surface while forming said etch resistant material over said conductive layer in said recess.

30. The method of claim 25 wherein said etch resistant layer comprises a polymer.

31. The method of claim 25 wherein said wafer assembly comprises a layer of oxide and said recess is formed in said oxide layer.

32. A method used to form a semiconductor device having a capacitor, comprising:

a) placing a semiconductor wafer assembly into a chamber of a plasma source, said wafer assembly comprising a layer of insulation having at least one contact therein and a surface, and further comprising a conductive layer over said surface and in said contact;

b) in said chamber, forming a layer of etch resistant material within said contact over said conductive layer, said etch resistant material not forming over said surface.

33. The method of claim 32, further comprising:

c) performing an etch using said etch resistant layer as a mask.

34. The method of claim 33 wherein said etch is performed in said chamber.

35. The method of claim 33, further comprising:

d) removing said etch resistant material from said contact subsequent to said step of performing said etch.

36. The method of claim 35 wherein said step of removing said etch resistant material from said contact is performed in said chamber.

37. The method of claim 35 wherein said step of forming said layer of etch resistant material removes said conductive layer from over said surface while forming said etch resistant material over said conductive layer in said contact.

38. The method of claim 35 wherein said etch resistant layer comprises a polymer.